European Initiative Projects Towards Exascale Computing

Chair: Jesus Carretero, Universidad Carlos III de Madrid, Spain

Outline:

- European Processor Initiative and EU Projects Towards Exascale Computing
- EPEEC: Europe toward High Coding Productivity for Exascale
- SparCity: Optimizing Sparse Computation and Graphs for Novel Parallel Architectures
- Round Table

European Processor Initiative and EU Projects Towards Exascale Computing

» Mario Kovac, University of Zagreb, Croatia

- September 3, 4:30 AM New York | 9:30 PM Lisbon | 10:30 PM Brussels | 4:30 PM Beijing

Project Aim: The European Processor Initiative (EPI) is a project currently implemented under the first stage of the Framework Partnership Agreement signed by the Consortium with the European Commission, whose aim is to design and implement a roadmap for a new family of low-power European processors for extreme scale computing, high-performance Big-Data and a range of emerging applications.

The project intends to deliver a high-performance, low-power processor, implementing vector instructions and specific accelerators with high bandwidth memory access. The EPI processor will also meet high security and safety requirements. This will be achieved through intensive use of simulation, development of a complete software stack and tape-out in the most advanced semiconductor process node. SGA1 will provide a competitive chip that can effectively address the requirements of the HPC, AI, automotive and trusted IT infrastructure markets.

EPEEC: Europe toward High Coding Productivity for Exascale

» Antonio Pena, Barcelona Supercomputing Center, Spain

- September 3, 4:30 AM New York | 9:30 PM Lisbon | 10:30 PM Brussels | 4:30 PM Beijing

Project Aim: EPEEC's main goal is to develop and deploy a production-ready parallel programming environment that turns upcoming overwhelmingly-heterogeneous exascale supercomputers into manageable platforms for domain application developers. The consortium will significantly advance and integrate existing state-of-the-art components based on European technology (programming models, runtime systems, and tools) with key features enabling 3 overarching objectives: high coding productivity, high performance, and energy awareness.

Project Objectives:

1. High coding productivity: A set of tools that can exploit the full power of the emerging hardware by turning them into manageable platforms for domain application developers;

2. High Performance: A programming environment with all relevant functionality at TRL8 for current pre-exascale systems and TRL4 for exascale platforms;

3. Energy Awareness: efficient and energy-aware management of hardware heterogeneity, both in terms of processing elements and memory subsystems further favouring coding productivity.

SparCity: Optimizing Sparse Computation and Graphs for Novel Parallel Architectures

» Didem Unat, Koç University, Turkey

- September 3, 4:30 AM New York | 9:30 PM Lisbon | 10:30 PM Brussels | 4:30 PM Beijing

Project Aim: The SparCity project aims at creating a supercomputing framework that will provide efficient algorithms and coherent tools specifically designed for maximising the performance and energy efficiency of sparse computations on emerging HPC systems, while also opening up new usage areas for sparse computations in data analytics and deep learning.

Project Objectives:

1. Develop a comprehensive application and data characterization mechanism and orchestrate an advanced and synergistic software optimization process, based on the state-of-the-art analytical and machine-learning-based performance and energy models;

2. Develop advanced node-level static and dynamic code optimizations designed for massive and heterogeneous parallel architectures with complex memory hierarchy and exploit mixed-precision opportunities for sparse computation;

3. Devise topology-aware partitioning algorithms and optimizations to minimize the communication overhead and boost the efficiency of system-level parallelism;

4. Create digital SuperTwins of supercomputers to evaluate and simulate what-if hardware scenarios and to gather real-time performance and energy intel from node- and system-level components for application optimization on the current and future hardware;

5. Demonstrate the effectiveness and usability of the SparCity framework by enhancing the computing scale and energy efficiency of four challenging real-life applications, namely, computational cardiology, social network analysis, bioinformatics and computer vision applications;

6. Deliver a robust, well-supported and documented SparCity framework into the hands of computational scientists, data analysts, and deep learning end-users from industry and academia.

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